ABSTRACT OF THE DISCLOSURE

The present invention provides a sensing scheme for semiconductor memory. N-type devices coupling between ground and a bit line and a bit line-bar of memory cells quickly discharge a bit line and a bit line-bar during non-accessing mode. During data accessing mode, one P-type device of an SRAM memory cell pulls up bit line or bit line-bar node slowly to minimize the inductive coupling noise and VDD, Ground bouncing, hence allows smaller amount of differential voltage input to the sense amplifier and results in lower power consumption. A self-timer counts the needed time and sends a signal to enable the current driven sense amplifier and to pull down the word line to avoid further pulling up the bit line or bit line-bar voltage and to reduce the power dissipation. A delay device coupling between the self-timer and bit line and bit line-bar avoids overlapping of pull-down and word line and reduces power leakage.